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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,507	09/19/2003	Jae-Hun Kim	8750-040	9186

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MARGER JOHNSON & McCOLLOM, P.C.  
1030 S.W. Morrison Street  
Portland, OR 97205

EXAMINER

PERKINS, PAMELA E

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/666,507

Applicant(s)

KIM ET AL.

Examiner

Pamela E Perkins

Art Unit

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XJ

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) 7-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,5 and 6 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/19/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This office action is in response to the filing of the election on 16 August 2004.

Claims 1-15 are pending; claims 7-15 have been withdrawn from consideration.

### ***Election/Restrictions***

Applicant's election without traverse of group I, claims 1-6 drawn to a semiconductor device in the reply filed on 16 August 2004 is acknowledged.

Claims 7-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention II, drawn to a method of manufacturing a semiconductor device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 16 August 2004.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (6,358,800) in view of Sugawara et al. (6,171,916).

Tseng discloses a MOS transistor where an isolation layer (114/116) formed at a predetermined region of a semiconductor substrate (110) to define an active region (Fig. 2A; col.2, line 64 thru col. 3, line 23); an upper trench region (118) formed in the active

region, the upper trench region (118) crossing the active region to divide the active region into two sub-active regions (Fig. 2B; col. 3, lines 34-29); a spacer (122) covering at least a pair of sidewalls of the upper trench region (118) that are adjacent to the active region (Fig. 2C & 2D; col. 3, lines 30-41); a lower trench region (124/126) formed under the upper trench region (118) surrounded by the spacer (122) (Fig. 2D & 2E; col. 3, lines 34-49); a pair of high concentration source/drain regions (136) formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region (118) respectively (Fig. 2I; col. 4, lines 18-33); a gate insulating layer (130) covering a bottom surface of the lower trench region (124/126) (Fig. 2F; col. 3, lines 50-55); and a gate electrode (132A) filling the lower trench region (124/126), and filling the upper trench region (118), surrounded by the spacer (122) (Fig. 2g & 2H; col. 4, lines 4-18).

Tseng further discloses the spacer comprising a first spacer (128) adjacent to the active region and a second spacer (122) adjacent to the isolation layer (114/116), the first spacer (128) having the same width as the second spacer (122) (Fig. 2J; col. 3, lines 33-60). Tseng also discloses a pair of low concentration source/drain regions (138) formed in the semiconductor substrate (110) under the first spacer (128), and formed in contact with sidewalls of the lower trench region (124/126) (Fig. 2J; col. 4, lines 34-42). Tseng does not disclose the gate insulating layer surrounding the trench region.

Sugawara et al. disclose a MOS transistor where an isolation layer (3) formed at a predetermined region of a semiconductor substrate to define an active region (col. 7,

lines 1-33); a trench region (6) formed in the active region, the trench region (6) crossing the active region to divide the active region into two sub-active regions (Fig. 2C; col. 7, lines 15-34); a pair of high concentration source/drain regions (12) formed at top surfaces of the sub-active regions that are located at both sides of the trench region (6) respectively (col. 7, lines 53-67); a gate insulating layer (21) covering the sidewalls and a bottom surface of the trench region (6) (Fig. 2D: col. 7, lines 34-42); and a gate electrode (22) filling the trench region (6), surrounded by the gate insulating layer (21) (Fig. 2F; col. 7, lines 43-51).

Since Tseng and Sugawara et al. are both from the same field of endeavor, MOS transistor, the purpose disclosed by Sugawara et al. would have been recognized in the pertinent art of Tseng. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Tseng by the gate insulating layer surrounding the trench region as taught by Sugawara et al. to reduce the resistance of the gate electrode (col. 2, lines 20-40).

Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Sugawara et al. as applied to claim 1 above, and further in view of Garcia (5,317,346).

Tseng in view of Sugawara et al. disclose the subject matter claimed above except the upper trench region has a greater width than the active region and the lower trench region has the same width as the active region.

Garcia discloses a MOS transistor where an isolation layer (54) formed at a predetermined region of a semiconductor substrate (51) to define an active region (Fig.

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4e; col. 4, line 65 thru col. 5, line 5); an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions (Fig. 4F; col. 4, lines 5-16); and a lower trench region (15) formed under the upper trench region (Fig. 4H; col. 4, lines 17-29). Garcia further discloses the upper trench region having a greater width than the active region and the lower trench region having the same width as the active region (Fig. 4H; col. 1, line 46 col. 2, line 19).

Since Tseng and Garcia are both from the same field of endeavor, a transistor, the purpose disclosed by Garcia would have been recognized in the pertinent art of Tseng. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Tseng by the upper trench region having a greater width than the active region and the lower trench region having the same width as the active region as taught by Garcia to increase strength (col. 1, lines 40-52).

#### ***Allowable Subject Matter***

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest the upper trench region having a width that is equal to or greater than the sum of twice width of the second spacer and the width of the active region.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

  
AMIR ZARABIAN  
TECHNOLOGY PATENT EXAMINER  
TECHNOLOGY CENTER 2800